4V Drive Nch MOS FET

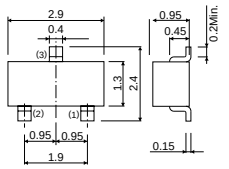
RK7002A

●Structure
Silicon N-channel MOS FET transistor

●Features
1) Low on-resistance.
2) High ESD
3) High-speed switching.
4) Low-voltage drive (4V).
5) Drive circuits can be simple.
6) Parallel use is easy.

●External dimensions (Unit : mm)

SST3



(1)Source
(2)Gate
(3)Drain

Each lead has same dimensions

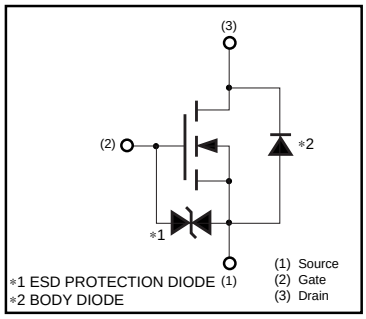
Abbreviated symbol : RKS

●Applications
Switching

●Packaging specifications

Type	Package	Taping
	Code	T116
	Basic ordering unit (pieces)	3000
RK7002A		◯

●Equivalent circuit



∗1 ESD PROTECTION DIODE
∗2 BODY DIODE

(1) Source
(2) Gate
(3) Drain

∗ A protection diode has been built in between the gate and the source to protect against static electricity when the product is in use.
Use the protection circuit when fixed voltages are exceeded.

●Absolute maximum ratings (Ta=25°C)

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DSS}	60	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	Continuous	I_D	±300	mA
	Pulsed	I_{DP} ∗1	±1.2	A
Source current (Body diode)	Continuous	I_S	200	mA
	Pulsed	I_{SP} ∗1	0.8	A
Total power dissipation		P_D ∗2	200	mW
Channel temperature		Tch	150	°C
Storage temperature		Tstg	−55 to +150	°C

∗1 Pw≤10μs, Duty cycle≤1%
∗2 With each pin mounted on the recommended land.

●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	Rth (ch-a) ∗	625	°C / W

∗ With each pin mounted on the recommended land.

●**Electrical characteristics** (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Gate leakage current	I_{GSS}	–	–	±10	μA	V_{GS}=±20V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)\ DSS}$	60	–	–	V	I_D=1mA, V_{GS}=0V
Drain cutoff current	I_{DSS}	–	–	1	μA	V_{DS}=60V, V_{GS}=0V
Gate threshold voltage	$V_{GS\ (th)}$	1	–	2.5	V	V_{DS}=10V, I_D=1mA
Drain-source on-state resistance	$R_{DS\ (on)}$*	–	0.7	1.0	Ω	I_D=300mA, V_{GS}=10V
		–	1.1	1.5		I_D=300mA, V_{GS}=4V
Forward transfer admittance	$\|Y_{fs}\|$*	0.2	–	–	S	V_{DS}=10V, I_D=300mA
Input capacitance	C_{iss}	–	33	–	pF	V_{DS}=10V V_{GS}=0V f=1MHz
Output capacitance	C_{oss}	–	14	–	pF	
Reverse transfer capacitance	C_{rss}	–	9	–	pF	
Turn-on delay time	$t_{d\ (on)}$*	–	6	–	ns	I_D=150mA, V_{DD}≒30V V_{GS}=10V R_L=200Ω R_G=10Ω
Rise time	t_r*	–	5	–	ns	
Turn-off delay time	$t_{d\ (off)}$*	–	13	–	ns	
Fall time	t_f*	–	80	–	ns	
Total gate charge	Q_g*	–	3	6	nC	V_{DD}≒30V V_{GS}=10V I_D=200mA
Gate-source charge	Q_{gs}*	–	0.6	–	nC	
Gate-drain charge	Q_{gd}*	–	0.5	–	nC	

* Pulsed

●**Body diode characteristics** (Source-Drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD}*	–	–	1.2	V	I_S=300mA, V_{GS}=0V

*Pulsed

●**Electrical characteristic curves**

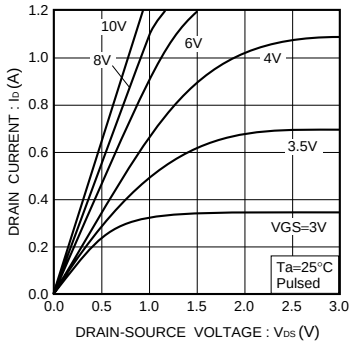


Fig.1 Typical output characteristics

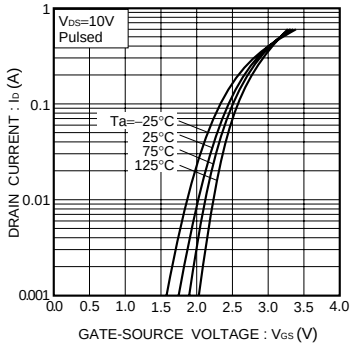


Fig.2 Typical transfer characteristics

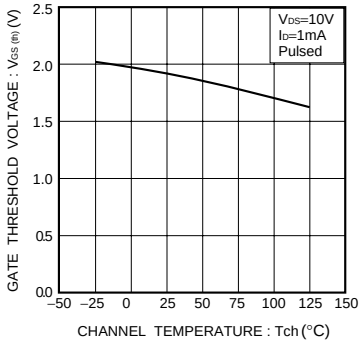


Fig.3 Gate threshold voltage vs. channel temperature

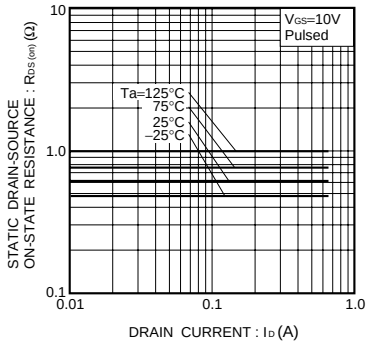


Fig.4 Static drain-source on-state resistance vs. drain current (I)

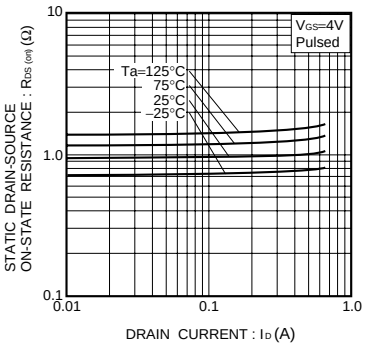


Fig.5 Static drain-source on-state resistance vs. drain current (II)

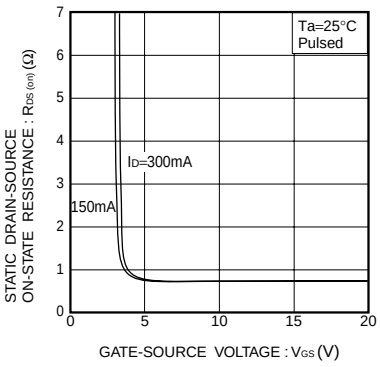


Fig.6 Static drain-source on-state resistance vs. gate-source voltage

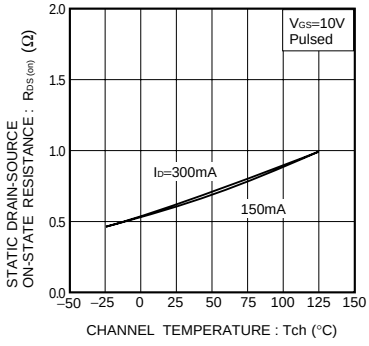


Fig.7 Static drain-source on-state resistance vs. channel temperature

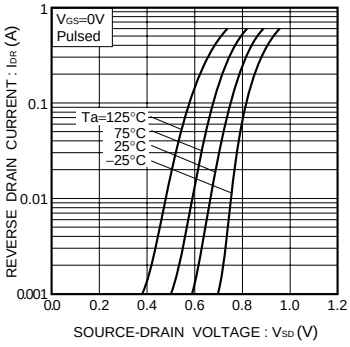


Fig.8 Reverse drain current vs. source-drain voltage (I)

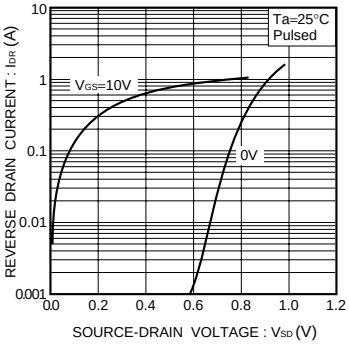


Fig.9 Reverse drain current vs. source-drain voltage (II)

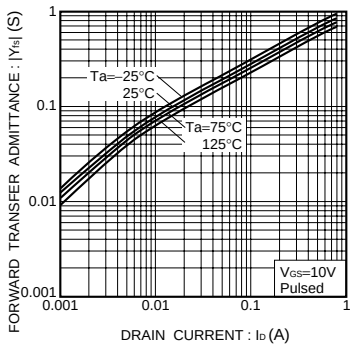


Fig.10 Forward transfer admittance vs. drain current

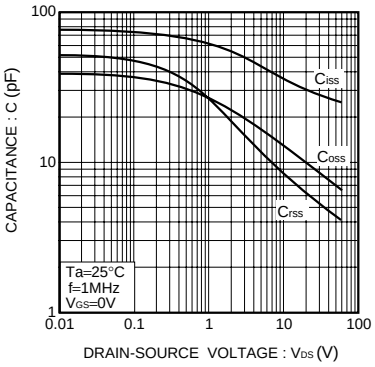


Fig.11 Typical capacitance vs. drain-source voltage

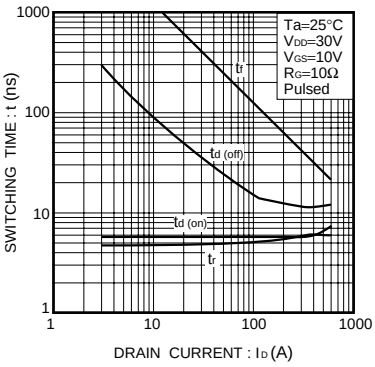


Fig.12 Switching characteristics (See Figures 13 and 14 for the measurement circuit and resultant waveforms)

●Switching characteristics measurement circuit

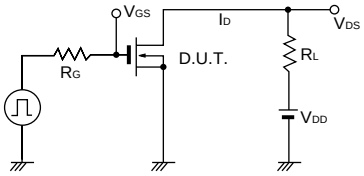


Fig.13 Switching time measurement circuit

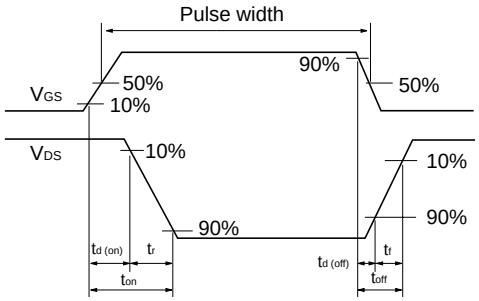


Fig.14 Switching time waveforms

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